FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: RCA 90419

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/623407

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/00524	03 March1999(03.03.99)	10March1998(10.03.98)

TITLE OF INVENTION: METHOD FOR DISPLAY MATRIX DISPLAY SCREEN WITH ALTERNATING SCANNING CONTROL IN ADJACENT GROUPS OF COLUMNS

532 Rec'd PCT/PTC 05 SEP 2000

APPLICANT(S) FOR DO/EO/US: Thierry Kretz; Hugues Lebrun; Bruno Mourey

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210). attached to Item 13
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. with references attached
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☐ Other items or information:

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

EL694405357US — "Express Mail" mailing no.

September 5, 2000 — Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Davida Fornarotto — Typed or printed name of person mailing application

Davida Fornarotto — Signature of person mailing application

PCTUS1/REV03

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/623407	PCT/FR99/00524	RCA 90419

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21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$970.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$840.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$670.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$96.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		840.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	4 - 20 =	0	x $18.00	
Independent claims	1 - 3 =	0	x $78.00	
Multiple Dependent Claims **(check if applicable).**			☐	

TOTAL OF ABOVE CALCULATIONS =	840.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).** ☐	
SUBTOTAL =	840.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +	
TOTAL NATIONAL FEE =	840.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐	
TOTAL FEES ENCLOSED =	840.00
Amount to be: refunded	$
charged	$ 840.00

☐ A check in the amount of to cover the above fees is enclosed.

☒ Please charge my Deposit Account No. 07-0832 in the amount of $840.00 to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 07-0832 A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

Sammy S. Henig
NAME

30,263
REGISTRATION NUMBER

September 5, 2000
DATE

SCANNED #17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Thierry Kretz; Hugues Lebrun; Bruno Mourey

Filed : Herewith

For : METHOD FOR DISPLAY MATRIX DISPLAY SCREEN WITH ALTERNATING SCANNING CONTROL IN ADJACENT GROUPS OF COLUMNS

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/FR99/00524 filed herewith, please enter the following amendments

IN THE TITLE:

Please amend the title of the application to be: -- METHOD FOR DISPLAY MATRIX DISPLAY SCREEN WITH ALTERNATING SCANNING CONTROL IN ADJACENT GROUPS OF COLUMNS--.

IN THE SPECIFICATION:

Page 1, lines 1-3, delete "PROCESS FOR DISPLAYING DATA ON A MATRIX DISPLAY WITH ALTERNATING ORDER OF SCANNING IN GROUPS OF ADJACENT COLUMNS" and insert -- METHOD FOR DISPLAY MATRIX DISPLAY SCREEN WITH ALTERNATING SCANNING CONTROL IN ADJACENT GROUPS OF COLUMNS --.

IN THE CLAIMS:

Please amend the claims as follows:

1.(AMENDED) Process for displaying data on a matrix display [consisting of] having N data lines and P selection lines at the intersections of which are situated the image points or pixels, and in which the N data lines are grouped into P' blocks of N' data lines each ($N = P \times N'$), each block receiving in parallel one of the P' data signals which is demultiplexed on the N' lines of [the] said block, [characterized in that] wherein, alternately , according to the selection lines, the scanning of the N' data lines of a block is carried out from 1 to N' [or] and from N' to 1.

2.(AMENDED) Process according to Claim 1, [characterized in that] wherein the scan from 1 to N' then from N' to 1 is carried out every second selection line.

3.(AMENDED) Process according to Claim 1, [characterized in that] wherein the scan from 1 to N' then from N' to 1 is carried out for four successive selection lines, the scan being carried out in a first direction for two successive selection lines and in a second direction for the other two succeeding selection lines.

4.(AMENDED) Circuit for implementing the process according to [any one of Claims 1 to 3, characterized in that it consists of] Claim 1, including at least one programmable logic circuit associated with a line counter determining the reversal of the direction of scan.

IN THE ABSTRACT

Please amend the Abstract as shown on the attached page.

REMARKS

The title has been amended to conform with the translated title of the published application (WO99/46753).

The above claim amendments have been made to eliminate multiple dependencies and to meet the requirements of the United States Patent and Trademark Office.

To meet the requirements of the United States, the Abstract (as originally filed during the prosecution of the PCT application) is added. Reference indicia has been deleted.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
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September 5, 2000

ABSTRACT

The present invention relates to a process for displaying data on a matrix display consisting of N data lines and P selection lines at the intersections of which are situated the image points or pixels. The N data lines are grouped into P blocks of N′ lines where N = P × N′. Each block receives in parallel one of the P′ data signals which is demultiplexed on the N′ lines of the said block. The scanning of the N′ data lines of a block is carried out from 1 to N′ or from N′ to 1, alternately, according to the selection lines.

PROCESS FOR DISPLAYING DATA ON A MATRIX DISPLAY WITH ALTERNATING ORDER OF SCANNING IN GROUPS OF ADJACENT COLUMNS

The present invention relates to a process for displaying data on a matrix display, more particularly a matrix display consisting of N data lines and M selection lines at the intersections of which are situated image points or pixels, and in which the N data lines are grouped into P blocks of N' data lines each.

Among matrix displays, the liquid crystal screens used in direct viewing mode or in projection mode are in particular known. These screens are, in general, composed of a first substrate comprising selection lines, hereinafter referenced lines, and data lines, hereinafter referenced columns, at the intersections of which are situated the image points and of a second substrate comprising a back electrode, the liquid crystals being inserted between the two substrates. The image points consist in particular of pixel electrodes connected across switching circuits, such as transistors, to the selection lines and the data lines. The selection lines and the data lines are respectively connected to peripheral control circuits generally referred to as "drivers". The line drivers scan the lines one after another and close the switching circuits, that is to say turn on the transistors of each line. On the other hand, the column drivers apply a cue to each data line, that is to say they charge the electrodes of the selected pixels and modify the optical properties of the liquid crystal contained between these electrodes and the back electrode, thus allowing the formation of images on the screen. When the matrix display comprises a limited number of lines and columns, each column is connected by its own connection line to the column drivers of the screen.

In the case of a screen with high definition, the principle of multiplexing is used between the outputs of the column driver and the columns of the screen in such a way as to reduce the number of tracks at the input of the cell. Thus, in French patent application No. 96 00259 filed on 11 January 1996 in the name of the Applicant, there is described a column control circuit of a matrix display such as represented in Figure 1. In this case, the columns are grouped into P blocks 1 of N' columns, i.e. 9 columns C1, C2, C3 ... C9 in the embodiment represented. Each block consists of transistors 3, one of the electrodes of which is linked to a column and the other electrode of which is connected to the same electrode of the other transistors of the block, together these electrodes being connected to a video input referenced DB1 for the first block, DB2 for the second block, DBP for the last block. The gates of the transistors 3 each receive a demultiplexing signal DW1, DW2, DW3 ... DW9. Each block exhibits the same structure.

The timing diagrams for the voltages read off from the successive columns of one and the same block 1 receiving a video signal DB1 to DBP are represented in Figure 2. In plotting these timing diagrams it has been assumed that the DC and AC voltage errors introduced by column-line-column coupling (referenced 2 in Figure 1), the origin of which was described in French patent No. 96 00259 filed on 11 January 1996, are perfectly corrected by the compensation circuit presented in this same patent. Each timing diagram represents a line time of a given column (1 to 9) of a block connected for example to DB1. In the case of a line time of 32 µs, the signals can be broken down as follows:

1. Precharging of all the columns of the matrix — 4 µs
2. Stabilization of the precharge — 0.5 µs
3. Sampling of the video over the 9 columns of the block DB — 9 × 2 µs
4. Equalization between column and pixel — 7.5 µs

5. Deselection of the line 2 µs.

These diagrams show that the voltage of the columns and hence the RMS voltage across the terminals of the liquid crystal cell, the electrodes of which are respectively the column and the electrode CE opposite, changes according to the order of sampling of the columns of a block connected to DBP. Now, since the dielectric constant of the liquid crystal varies as a function of the voltage applied to its terminals, the columns of one and the same block receiving a signal DBi do not therefore exhibit the same charging capacity. Consequently, the coupling between the gates of the sampling transistors and the columns of one and the same block receiving the signal DBi increases as a function of the order of sampling of the columns, this introducing a DC error of several tens of mV between the first column sampled in the block receiving the signal DBi and the last.

The purpose of the present invention is to propose a process for displaying data on a matrix display which makes it possible to remedy this drawback.

Accordingly, the subject of the present invention is a process for displaying data on a matrix display consisting of N data lines and M selection lines at the intersections of which are situated the image points or pixels, and in which the N data lines are grouped into P blocks of N′ data lines each (N = P × N′), each block receiving in parallel one of the P data signals which is demultiplexed on the N′ lines of the said block, characterized in that, alternately according to the selection lines, the scanning of the N′ data lines of a block is carried out from 1 to N′ or from N′ to 1.

According to one embodiment of the present invention, the scan from 1 to N′ then from N′ to 1 is carried out every second selection line.

According to another embodiment which makes it possible to obtain the same continuous level on all the

columns, the scan from 1 to N' then from N' to 1 is carried out for four successive selection lines, the scan being carried out in a first direction for two successive selection lines and in a second direction for the other two succeeding selection lines.

The present invention also relates to a circuit for implementing the above process. This circuit consists of at least one programmable logic circuit associated with a line counter determining the reversal of the direction of scan.

Other characteristics and advantages of the present invention will become apparent from reading the description given hereinbelow, this description being given with reference to the drawings appended hereto in which:

- Figure 1 already described is a schematic representation of a matrix display in which the columns are grouped into blocks, and which will be used for the implementation of the present invention.

- Figure 2, already described, represents the timing diagrams, over a line time, of the odd numbered columns of a block DB consisting of 9 columns, and

- Figure 3 is a schematic representation of a circuit used to implement the present invention.

To simplify the description hereinbelow, in the figures the same elements bear the same references.

The process in accordance with the present invention is applied chiefly to a matrix display of the type represented in Figure 1. This display consists of N data lines or columns and M selection lines at the intersections of which are situated the image points or pixels (not represented). The N columns are grouped into P blocks 1 of N' columns each. By way of example, in Figure 1 is represented a block of 9 columns. Usually for a screen used for a video display, the column control circuit will contain 80 blocks of 9 adjacent columns and will operate with a sampling frequency of around 500 kHz. As represented in Figure 1, each block 1 receives in parallel one of the

P or 80 data signals which is demultiplexed by the signals DW1 to DW9 on the N' or 9 columns of a block. In accordance with the present invention, to avoid the DC error between the columns of one and the same block, due to the coupling between the gate of the sampling transistor and the column, which error changes as a function of the order of sampling of the columns, for the selection line L1, each block 1 is scanned successively from line C1 to C9 by applying sampling pulses DW1 to DW9, and signals such as represented in Figure 2 are obtained on each column C1 to C9. Then, for the next line L2 each block is scanned, beginning from column C9, towards column C1 by applying sampling pulses from DW9 to DW1 in such a way as to reduce the DC error as explained in the introduction with reference to Figure 2.

According to a variant embodiment of the process which makes it possible to obtain the same continuous level on all the columns, the scan is reversed by reversing the arrival of the sampling pulses every second line out of four lines according to the following table:

Line	Frame 1	Frame 2	Frame 3
1	DW1 to 9	DW1 to 9	DW1 to 9
2	DW1 to 9	DW1 to 9	DW1 to 9
3	DW9 to 1	DW9 to 1	DW9 to 1
4	DW9 to 1	DW9 to 1	DW9 to 1
5	DW1 to 9	DW1 to 9	DW1 to 9
6	DW1 to 9	DW1 to 9	DW1 to 9

It should be noted in the above table that, unlike what happens with the video data which are reversed on the image points from one frame to another so as to avoid the marking of the cell, the direction of scanning of the signals DWj is preserved from one frame to another for a given selection line so as to avoid the AC error which would result therefrom.

The present invention also relates to a circuit making it possible to implement this process. This circuit consists of at least one programmable logic circuit associated with a line counter determining the reversal of the direction of scan.

An exemplary circuit making it possible to generate the scan of each block receiving the demultiplexing signals DW1 to DWN' from 1 to N' then from N' to 1 every 2 lines is represented in Figure 3. This circuit is based on a programmable logic circuit EPLD 10 which governs the order of dispatch of the video data (DB) to the cell and the direction of scan of the signals DW (j = 1 to N') in a block receiving a given signal DB (i = 1 to P) according to the bit of rank 2 of the address at the output of the line counter (11) in the case of the example represented; that is to say:

- if the bit of rank 2 at the output of the line counter (11) equals 0 (xxxxxx00 or xxxxxx01), the words DWj' are read from 1 to N' and the P video data, stored in the line memory 13, are transferred to a D/A control circuit 14, i.e. a digital/analogue converter upstream of the cell in the order of the DWs according to the table below:

DW	DB	Column number
1	k with k integer and $1 \leq k \leq P$	$N' \times (k-1) + 1$ with k integer and $1 \leq k \leq P$
2	k with k integer and $1 \leq k \leq P$	$N' \times (k-1) + 2$ with k integer and $1 \leq k \leq P$
N'	k with k integer and $1 \leq k \leq P$	$N' \times (k-1) + N'$ with k integer and $1 \leq k \leq P$

- otherwise the words DWj are read from N' to 1 and the P video data are transferred to the D/A control circuit 14 in the order indicated in the table below:

DW	DB	Column number
N′	k with k integer and $1 \leq k \leq P$	N′ × (k-1) + N′ with k integer and $1 \leq k \leq P$
2	k with k integer and $1 \leq k \leq P$	N′ × (k-1) + 2 with k integer and $1 \leq k \leq P$
1	k with k integer and $1 \leq k \leq P$	N′ × (k-1) + 1 with k integer and $1 \leq k \leq P$

In more detail, the signal referenced Preset at the output of the line counter 11 controlled by the line clock CL is dispatched respectively to a counter modulo N′ 15 and to a counter DW 16. The counter modulo N′ 15 is controlled by the data clock CD and operates so that:

If Preset = 0 the video data are transferred as they are.

If Preset ≠ 0 N′ + 1 - the video data are transferred.

Likewise, the counter DW 16 is controlled by the clock of the DWs DWC and operates as follows:

If Preset = 0 the words are transferred in the normal order.

If Preset ≠ 0 the words are transferred in the reverse order.

This cue at the output of the counter DW is dispatched to a level shifting circuit 17 and returned to the counter modulo N′ 18.

It is obvious to the person skilled in the art that this is merely one particular embodiment which can be modified without departing from the claims.

CLAIMS

1. Process for displaying data on a matrix display consisting of N data lines and P selection lines at the intersections of which are situated the image points or pixels, and in which the N data lines are grouped into P′ blocks of N′ data lines each (N = P × N′), each block receiving in parallel one of the P′ data signals which is demultiplexed on the N′ lines of the said block, characterized in that, alternately according to the selection lines, the scanning of the N′ data lines of a block is carried out from 1 to N′ or from N′ to 1.

2. Process according to Claim 1, characterized in that the scan from 1 to N′ then from N′ to 1 is carried out every second selection line.

3. Process according to Claim 1, characterized in that the scan from 1 to N′ then from N′ to 1 is carried out for four successive selection lines, the scan being carried out in a first direction for two successive selection lines and in a second direction for the other two succeeding selection lines.

4. Circuit for implementing the process according to any one of Claims 1 to 3, characterized in that it consists of at least one programmable logic circuit associated with a line counter determining the reversal of the direction of scan.

ABSTRACT

PROCESS FOR DISPLAYING DATA ON A MATRIX DISPLAY

The present invention relates to a process for displaying data on a matrix display consisting of N data lines (C1, C2, C3, ...) and P selection lines (L1, L2, L3, L4, ...) at the intersections of which are situated the image points or pixels (2).

The N data lines are grouped into P blocks (1) of N′ lines (1 to Cg) where N = P × N′, each block (1) receives in parallel one of the P′ data signals (DB1, ...) which is demultiplexed (DW1, DW2, DW3, ... DW9) on the N′ lines of the said block. The scanning of the N′ data lines of a block is carried out from 1 to N′ or from N′ to 1, alternately according to the selection lines.

Application to matrix displays such as LCD screens.

Fig. 1

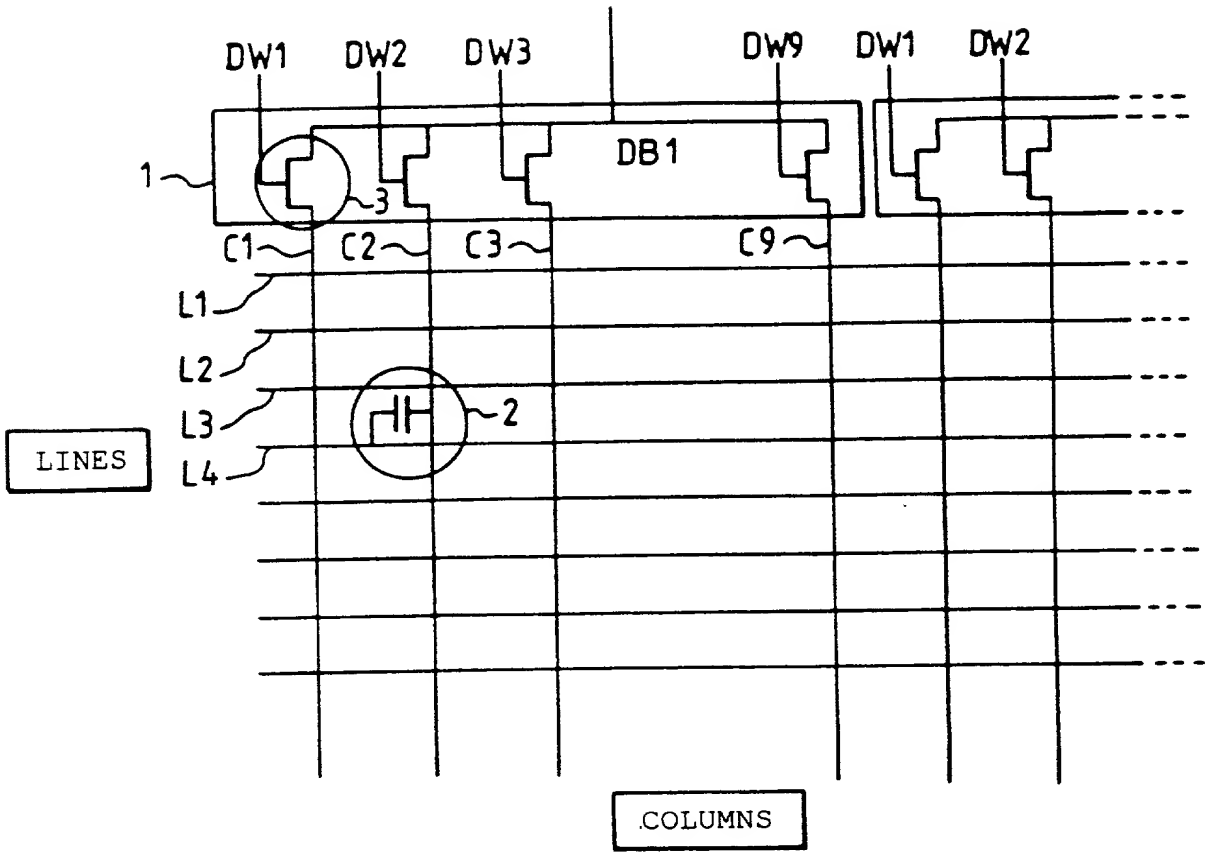

DW1
DW2
DW3
DW9
DW1
DW2
DB1
1
3
C1
C2
C3
C9
L1
L2
L3
L4
2
LINES
COLUMNS

FIG.1

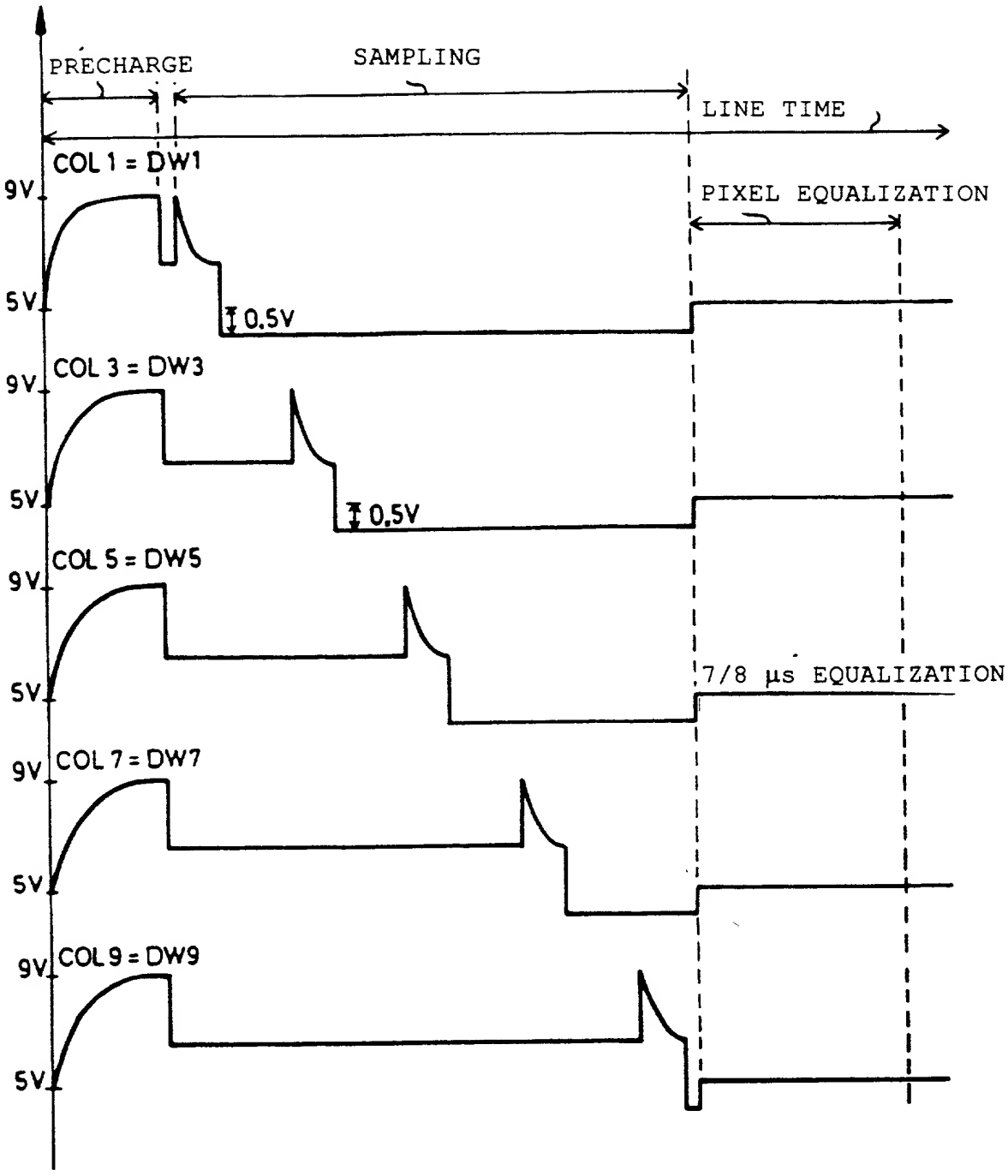
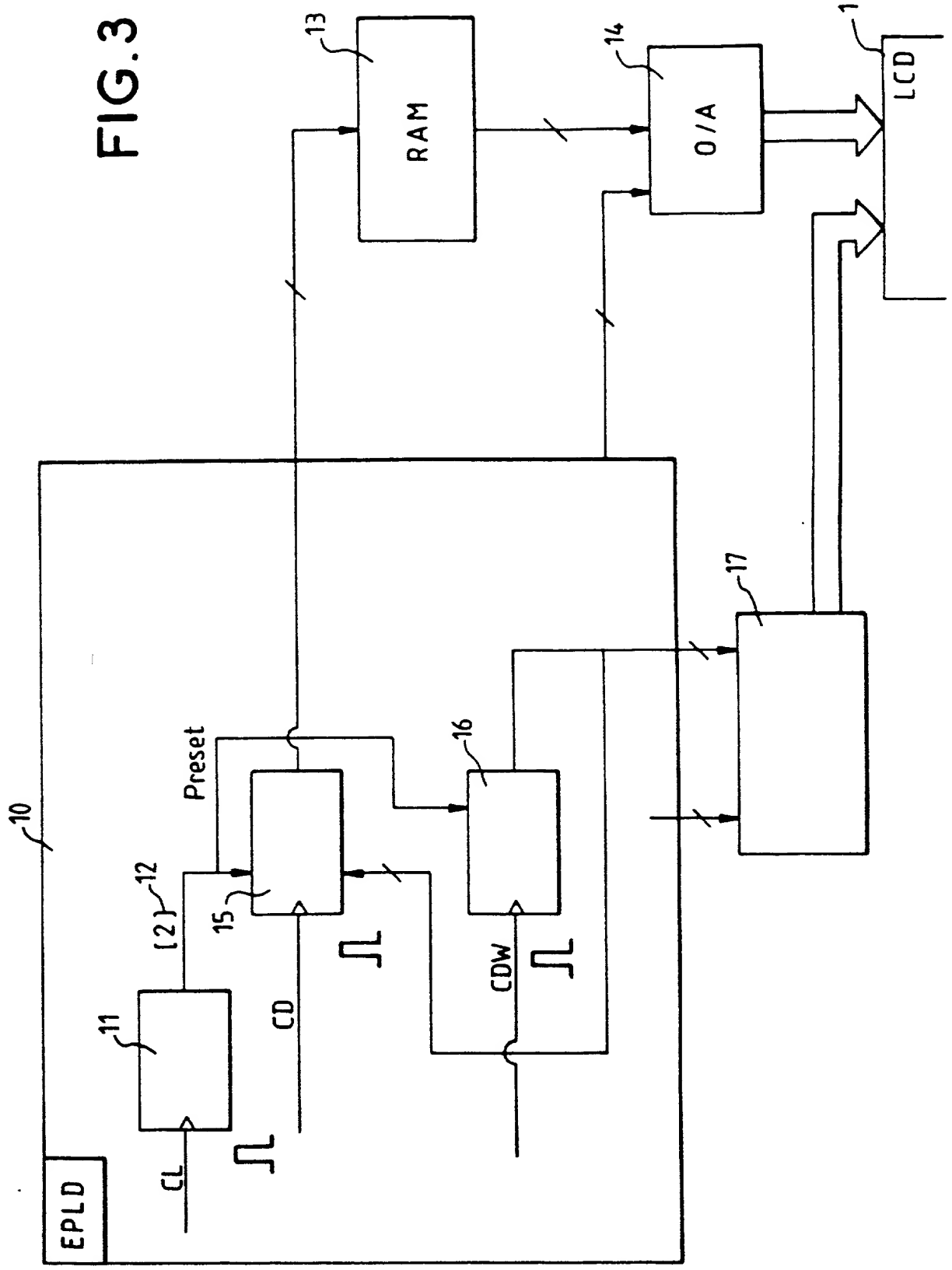

PRECHARGE
SAMPLING
LINE TIME
COL 1 = DW1
9V
5V
0.5V
PIXEL EQUALIZATION
COL 3 = DW3
9V
5V
0.5V
COL 5 = DW5
9V
5V
7/8 µs EQUALIZATION
COL 7 = DW7
9V
5V
COL 9 = DW9
9V
5V

FIG.2

FIG.3



DECLARATION FOR UNITED STATES PATENT APPLICATION,
POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"PROCESS FOR DISPLAYING DATA ON A MATRIX DISPLAY WITH ALTERNATING ORDER OF SCANNING IN GROUPS OF ADJACENT COLUMNS"

the specification of which
(CHECK ONE) ( ) is attached hereto.
(xx) was filed on March 9, 1999, Application Serial. No. PCT/FR99/00524 and was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
9802919	FR	March 10, 1998	xx	

I hereby claim the benefit under 35 USC 120 of any US Application(s) listed below, and, insofar as the subject matter of each of the claims of this Application is not disclosed in the prior US application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

Serial No.: Filed:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under of 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Joseph S. Tripoli (Reg. No. 26,040), Joseph J. Laks (Reg. No. 27,914), Dennis H. Irlbeck (Reg. No. 26,372), Eric Herrmann (Reg. No. 29,169) Telephone: (609) 734-9754

Address all correspondence to Joseph S. Tripoli, Patent Operations - GE and RCA - Licensing Management Operation, Inc. - CN 5312 - Princeton, New Jersey 08543-0028.

Signature: Thierry KRETZ Date: 1st August, 2000.
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